1. A neuromorphic circuit for a Hebbian synapse including an alpha function circuit, an NMDA ion channel circuit, and a non-NMDA ion channel circuit having a conductance level, comprising:

a control circuit for coupling with the non-NMDA ion channel circuit to control the conductance level of the non-NMDA ion channel circuit in response to a voltage level on a synapse calcium capacitor that is indicative of a calcium concentration in the synapse circuit.

2. The circuit according to claim 1, wherein the control circuit includes a counter.

3. The circuit according to claim 1, wherein the control circuit includes a counter for loading the conductance level of the synapse and decrementing, incrementing, or leaving the same, the conductance level.

4. The circuit according to claim 1, wherein the control circuit includes a threshold circuit coupled to the synapse calcium concentration capacitor for providing potentiation charge and depression charge signals.

5. The circuit according to claim 4, wherein a state of the potentiation charge signal corresponds to a voltage on the synapse calcium concentration capacitor in comparison to a first voltage threshold.

6. The circuit according to claim 5, wherein a state of the depression charge signal corresponds to the voltage on the synapse calcium concentration capacitor in comparison to a second voltage threshold.

7. The circuit according to claim 4, wherein the control circuit further includes a potentiation discharging and charging circuit coupled to the threshold circuit for charging a potentiation capacitor when the voltage on the synapse calcium concentration capacitor exceeds the first threshold.

8. The circuit according to claim 7, wherein the control circuit further includes a depression discharging and charging circuit coupled to the threshold circuit for charging a depression cacpacitor when the voltage on the synapse calcium concentration capacitor exceeds the second threshold.

9. The circuit according to claim 8, wherein the control circuit further includes a potentiation detector circuit for providing a potentiation signal to the counter having a state that corresponds to a voltage level on the potentiation capacitor and a depression detector circuit for providing a depression signal to the counter having a state that corresponds to a voltage level on the depression capacitor.

10. The circuit according to claim 9, wherein the states of the potentiation signal and the depression signal can modify the conductance level of the synapse.

11. The circuit according to 9, wherein the control circuit further includes an up/down counter circuit that loads the conductance level of the synapse, and wherein the states of the potentiation signal and the depression signal determine whether the counter increments, decrements, or leaves the same, the synapse conductance level.

12. The circuit according to claim 11, wherein the counter is an up/down counter having a counter value of at least six bits corresponding to the conductance level of the synapse.

13. The circuit according to claim 9, wherein the potentiation capacitor has a smaller capacitance than the depression capacitor.

14. A neurpmorphic Hebbian synapse circuit including an NMDA ion channel circuit and a non-NMDA ion channel circuit, comprising:

a control circuit for adjusting the synapse conductance level in response to a voltage level on a synapse concentration capacitor, the control circuit including

a threshold circuit providing a potentiation charge signal having a state corresponding to a comparison of a voltage on the calcium concentration capacitor to a first voltage threshold that corresponds to long term depression of the synapse, the threshold circuit further providing a depression charge signal having a state corresponding to a comparison of the voltage on the calcium concentration capacitor and a second voltage threshold that corresponds to long term potentiation of the synapse;

a potentiation discharging and discharging circuit coupled to the threshold circuit for selectively charging a potentiation capacitor based upon the state of the potentiation charge signal and for selectively charging a depression capacitor based upon the state of the depression charge signal;

a potentiation detector circuit coupled to the potentiation discharging and charging circuit for providing a potentiation signal having a state determined by a voltage level on the potentiation capacitor;

a depression detector circuit coupled to the depression discharging and charging circuit for providing a depression signal having a state determined by a voltage level on the depression capacitor; and

a counter for loading the conductance level of the synapse and incrementing, decrementing, or leaving the same, the conductance level based upon the states of the potentiation signal and the depression signal.

15. The circuit according to claim 14, wherein the counter has a counter value of at least six bits.

16. The circuit according to claim 14, wherein the counter is time shared between further synapses.

17. The circuit according to claim 14, wherein the potentiation capacitor has a smaller capacitance than the depression capacitor.

18. A method for controlling a neuromorphic Hebbian synapse circuit having a synapse calcium concentration capacitor that charges in response to stimuli and a synapse conductance

level that corresponds to a conduction state of electrical pathways in the synapse circuit, each of the electrical pathways having a switching element that determines the conduction state of the electrical pathway, the method comprising:

controlling the conduction state of the switching elements by

providing a potentiation charge signal having a state corresponding to a comparison of a voltage on the calcium concentration capacitor to a first voltage threshold that corresponds to long term depression of the synapse;

providing a depression charge signal having a state corresponding to a comparison of the voltage on the calcium concentration capacitor and a second voltage threshold that corresponds to long term potentiation of the synapse;

selectively charging a potentiation capacitor based upon the state of the potentiation charge signal;

selectively charging a depression capacitor based upon the state of the depression charge signal;

providing a potentiation signal having a state determined by a voltage level on the potentiation capacitor;

providing a depression signal having a state determined by a voltage level on the depression capacitor; and

incrementing, decrementing, or leaving the same, the synapse conductance level based upon the states of the potentiation signal and the depression signal.

19. The method according to claim 18, wherein the synapse conductance level is defined by at least six bits.

20. The method according to claim 18, further including selecting a capacitance value for the depression capacitor that is less than that of the potentiation capacitor.